

Claim 1 recites features that are neither disclosed nor suggested in the prior art of record. Yonemitsu discloses reproducing an image having a reduced resolution by processing a coded bit stream of normal resolution. Yonemitsu does not disclose, however, reproducing a frame of image data using only one of the two fields that form a frame. The examiner suggests that Yonemitsu discloses selecting one of two fields forming each frame at figure 9a, element 52. However, Yonemitsu's figure 9a is a block diagram of an encoder. [Yonemitsu, col. 16, Ins. 23-24.] Applicant's claim 1 does not recite encoding image data. Claim 1 recites a method for displaying frames of encoded image data. Thus, even if Yonemitsu's element 52 did select one of two fields that form a frame, it would do so in an encoding process and not in a decoding process.

Moreover, Yonemitsu's element 52 does not operate to select one of two fields that form a frame in any event. Indeed, the element 52 provides an output signal that includes data from both fields that form the frame, as is illustrated in figure 10(B). [Yonemitsu, col. 5, Ins. 10-15, see also fig. 10(B).]

In addition, Yonemitsu does not disclose taking the output from element 52 and adding zero values to it, as is recited by claim 1. The examiner has combined features of Yonemitsu's encoder (figure 9(B), element 52) with Yonemitsu's decoder (figure 15, elements 72 and 92). Thus, Yonemitsu does not disclose performing the steps recited in claim 1, which steps include decoding and displaying encoded image data.

The examiner correctly notes that Yonemitsu's element 92 does not perform adding zero values after the DCT coefficients of each field block as recited in amended claim 1. The examiner states, however, that this step would have been obvious in view of Matsushima which teaches adding zeros to get the larger size blocks required for a desired display output format. However, applicant's invention must be considered as a whole and the relevant inquiry is whether applicant's invention as a whole is made obvious in view of the combined prior art. As indicated above, applicant's invention, as recited in claim 1, for example, recites selecting one of two fields that form each frame, adding zero values after the DCT coefficients of the selected field and performing the inverse DCT of the compensated DCT coefficients to obtain image data. Yonemitsu simply does not disclose reproducing a frame of image data using only one of two fields that form a frame. Yonemitsu does not select one of

two field, and indeed Yonemitsu's element 15 provides an output that includes data from both fields that form the frame. Matsushima does not cure the missing defects of Yonemitsu. Thus, even though Matsushima teaches adding zeros or taking away zeros to enlarge or reduce an image, this teaching, even combined with Yonemitsu, does not make applicant's invention obvious when applicant's invention is considered as a whole. Thus, neither the combined teachings of Yonemitsu and Matsushima disclose selecting a single field among two fields, adding the zero values to the selected field and reproducing the image data utilizing the selected field. Thus, the combined teachings of Yonemitsu and Matsushima do not make out a *prima facie* case of obviousness under the provisions of 35 U.S.C. § 103.

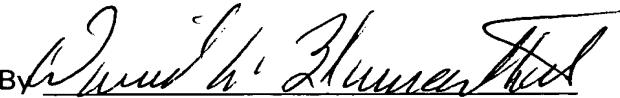
The examiner's rejection of claim 3 also is respectfully traversed for the reasons discussed above. Further, amended claim 3 recites, among other features, alternatively selecting one of an odd field and an even field that form each frame. This feature is neither disclosed nor suggested in the prior art of record. Thus, applicant believes that claim 3 is in condition for allowance.

Claims 2 and 4 are dependent on claims 1 and 3, respectively. Thus, the examiner's rejection of claims 2 and 4 is likewise traversed.

Claim 5 recites, among other features, an apparatus for displaying frames of a dynamic image including a selecting device that selects one of two fields forming each picture frame. Claim 5 further recites a DCT coefficient addition device that adds zero values after the DCT coefficients of each field block in the selected field. As discussed above, these features are neither disclosed nor suggested in the prior art of record. Thus, the examiner's rejection of claim 5 is respectfully traversed. Claims 6 and 7 are dependent on claim 5. Thus, the examiner's rejection of claims 6 and 7 is likewise traversed.

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance. Re-examination and reconsideration of the application, as amended, and allowance of the claims at an early date is respectfully requested.

Respectfully submitted,

By 

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